REMARKS

Favorable reconsideration of this application, in light of the following remarks, is respectfully requested.

Claims 1-16 and 18-23 are pending in this application. Claims 17, 24 and 25 have been canceled by a previous amendment.

RESPONSE TO AMENDMENT

Initially, Applicants note that the Examiner has refused to enter amendments made to the specification and drawings; however, Applicants, on the record, object to the Examiner's arbitrary refusal of entering the amendments. The Examiner does **not have** the arbitrary discretion to enter or not enter amendments, when the amendments are made in response to a **non-final office action**. The Examiner must enter the amendments, and if warranted, object or reject the amendments in the subsequent office action.

With regard to paragraph [0014], claim 16 recites that "test signals [are received] from a core circuit on the chip via a plurality of signal input/output pins." In other words, the I/O pins receives test signals. The test signals coming from the core circuit. Please note, no where in the specification, claims, and/or drawings does it teach or recite that the I/O pins are connected to the core circuit, as alleged by the Examiner.

DRAWINGS

The Examiner fallaciously refuses amendments made to FIG. 1. As discussed above, the Examiner does not have any discretion in deciding whether to enter or not enter amendments made in response to a non-final office action. Accordingly, entrance of the amendments to FIG. 1 is requested.

In addition, with all due respect, Applicants do not understand the Examiner's objection to amended FIG. 1 nor the Examiner's explanation thereof. For example, the Examiner alleges that the "test

signal" of claim 15 is the waveform of FIG. 3, and is not **an I/O pad signal**[.]" Applicants request that the Examiner re-review amendments made to paragraph [0014] and FIG. 1. Only reference numerals are added to paragraph [0014] and only **I/O pins** already disclosed in paragraph [0014] are added in FIG. 1. In addition, paragraph [0014] discloses that "Signals may be input to the **signal I/O pins** 101- 108 from a core circuit 110, and/or signals may be output from the **signal I/O pins** 101- 108 to the core circuit 110." (Emphasis added.)

In view of the remarks made above, Applicants request the Examiner to withdraw the Drawing objections and enter the amendments made to FIG. 1. Please see below for addition comments with regard to claim 16 and FIG. 1.

SPECIFICATION

Applicants maintain that paragraph [0019] **does not** require amendment. Applicants do not disagree that the number of inverters in order to oscillate must be an odd number. That fact is disclosed in paragraph [0020] of the present application. However, paragraph [0018] also discloses that unit delay circuits **may be** buffers, and if the unit delay circuits are buffers, then the number of inverters should be odd. Therefore, the present application also discloses that the unit delay circuits need not be buffers, if so, then the number inverts does not have be odd.

Applicants fail to understand why the Examiner insists that Applicants add amendments to the specification that potentially narrows the scope of the specification and claims: amendments that are also contrary to the original specification, and amendments that may potentially add new matter to the specification.

Accordingly, no amendments are required for paragraph [0019].

REJECTIONS UNDER 35 U.S.C. §112

Claim 16 is rejected under 35 U.S.C. §112, second paragraph. Applicants traverse this rejection.

In further view of the Examiner's drawing objection, the Examiner makes a follow-up rejection to claim 16. The Examiner states that he is unsure how a core circuit generates test signals as recited in claim 16, when "test signals are generated by the connected circuit groups of claim 15."

Applicants respectfully request that the Examiner re-read claim 15 and the disclosure of the present application, e.g., paragraph [0014]. For example, claim 15 recites, *inter alia*, "delaying test signals through a plurality of successively connected circuit groups." (Emphasis added.) No where in claim 15 does it recite that the test signals are generated in the successively connected circuit groups, only that the test signals are delayed in the successively connected circuit groups. Claim 16, which is a dependent claim, further defining claim 15, recites that the test signals are generated in core circuit. In other words, the test signals are generated in the core circuit (claim 16) and the test signals are delayed in the successively connected circuit groups (claim 15). The recitation in claims 15 and 16 are consistent with the specification, for example, paragraph [0014].

REJECTIONS UNDER 35 U.S.C. §102(b)

Claims 1-16 and 18-23 are rejected under §102(b) as being anticipated by Inoshita et at. (USP 6,477,115). Applicants traverse this rejection.

The Examiner alleges that Inoshita et al. teaches "there are no particular restrictions on the number of delay circuits provided to the delay monitor circuit 2g." The quoted passage means that the number of delay circuits in the delay monitor circuit 2g may be 2, 6, 9, 15, ...∞. However, independent claims 1, 8, and 15 recite, *inter alia*, "**each** circuit group including a **different number** of unit delay circuits." In other words, the number of unit delay circuits in each circuit group is different from each

other. Applicants draw the Examiner's attention paragraph [0015] of the present application, which clearly supports Applicants' position.

In addition, the Examiner cites a passage, which teaches a delay monitor circuit 2g may contain **any number** of delay circuits 9. Applicants submit that if "any number" is replaced with "different number," the following feature is recited, "**each** circuit group including [] **any number** of unit delay circuits." As the Examiner can see, the feature recited in claims 1, 8, and 15 is not what is taught by Inoshita et al.

Also, FIGS. 3, 6, 7, 11, 14, and 16 of Inoshita et al. each illustrate separate example embodiments. Even if TAPS 1-3 are a "pad" as alleged by the Examiner, the Examiner cannot combine separate components from different embodiments (FIGS. 14 and 16) and use the combination to reject the present claims under §102.

Accordingly, for at least the reasons given above, independent claim 1, 8, and 15 are patentable over Inoshita et al. Dependent claims 2, 5-7, 9, 12-14, 16-21 are also in a condition for allowance for respectively depending on an allowable independent claim.

REJECTIONS UNDER 35 U.S.C. §103(a)

Claims 3-4, 10-11, and 22-23 are rejected under §103(a) as being unpatentable over Inoshita in view of Patrie et al. (USP 6,219,305).

As discussed with respect to the patentability of independent claims 1, 8, and 15, Inoshita fails to teach all the features recited in independent claims 1, 8, and 15.

For at least the reasons given above, Applicants submit that dependent claims 3-4, 10-11 and 22-23 are patentable over Inoshita in view of Patrie et al. In addition, Patrie et al. fails to cure the deficiencies of Inoshita.

CONCLUSION

In view of the above remarks and amendments, the Applicants respectfully submit that each of the pending objections and rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below. If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge any underpayment or non-payment of any fees required under 37 C.F.R. §§ 1.16 or 1.17, or credit any overpayment of such fees, to Deposit Account No. 08-0750, including, in particular, extension of time fees.

Respectfully submitted,

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By: _____

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